

Figure 1 (Prior Art)

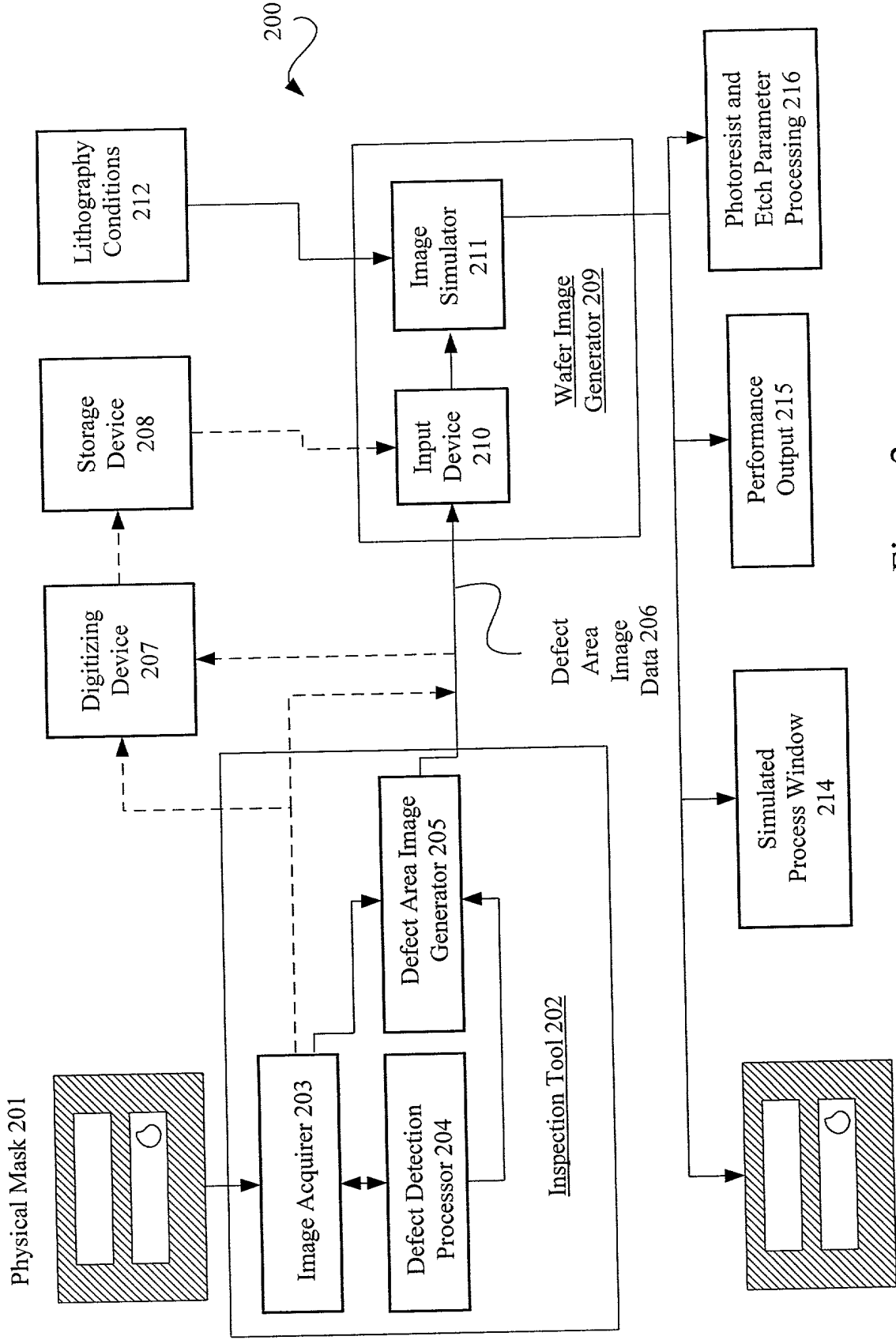


Figure 2

Simulated Wafer Image 213

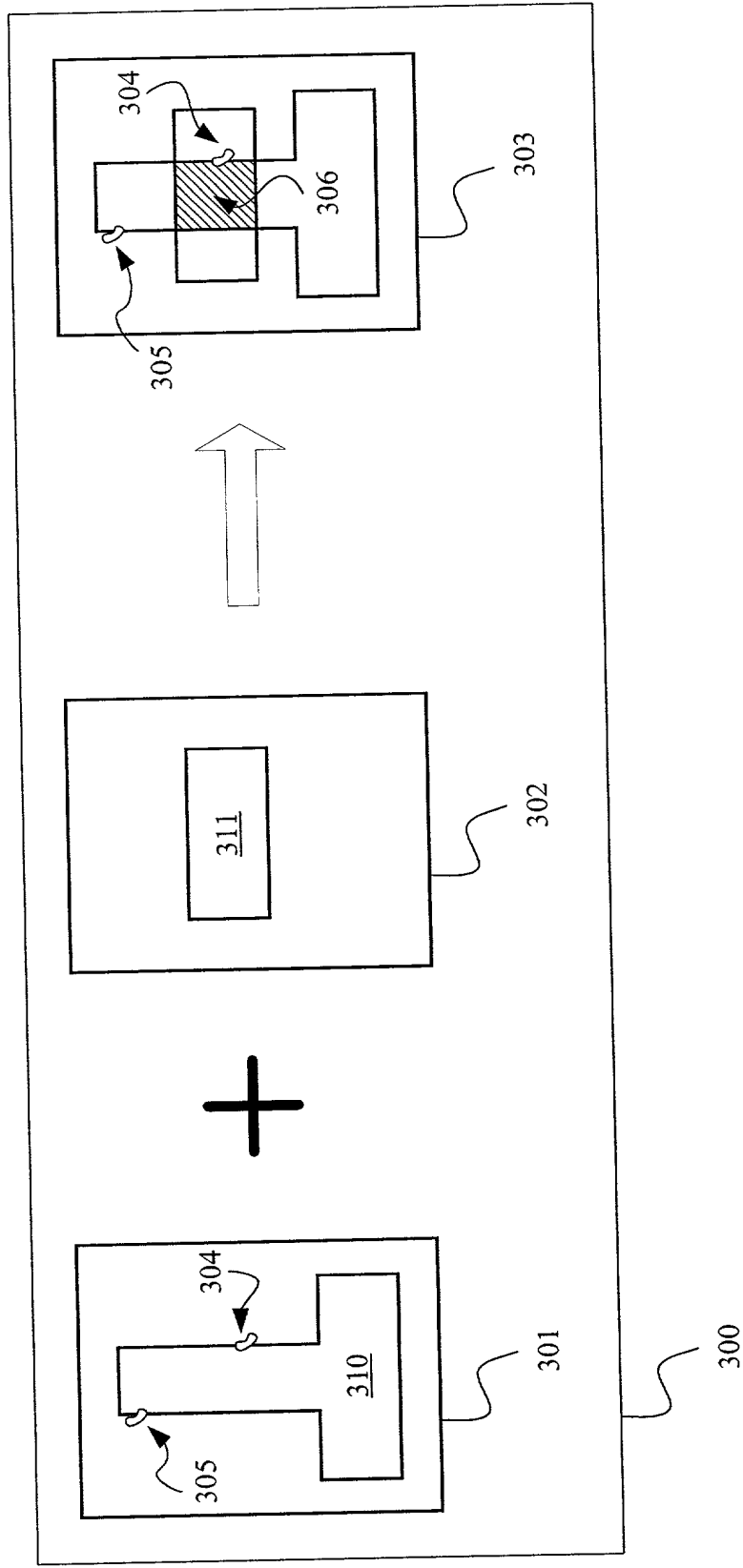


Figure 3

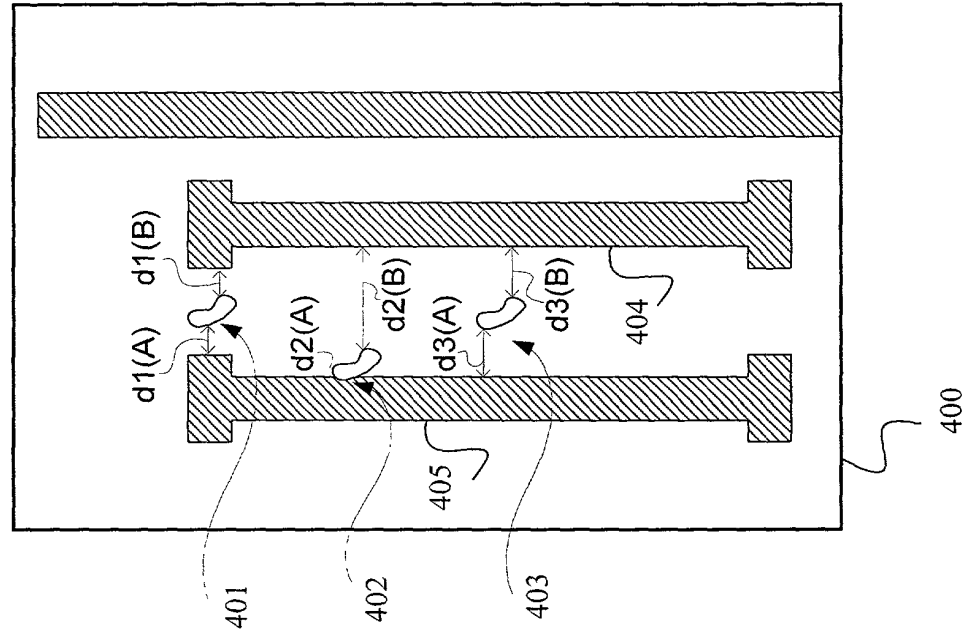


Figure 4B

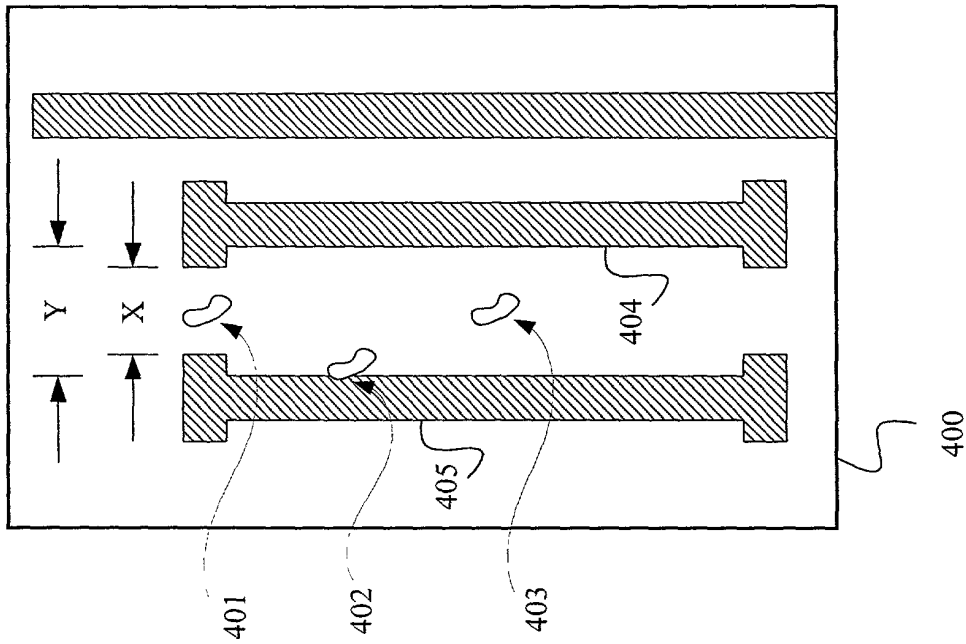


Figure 4A

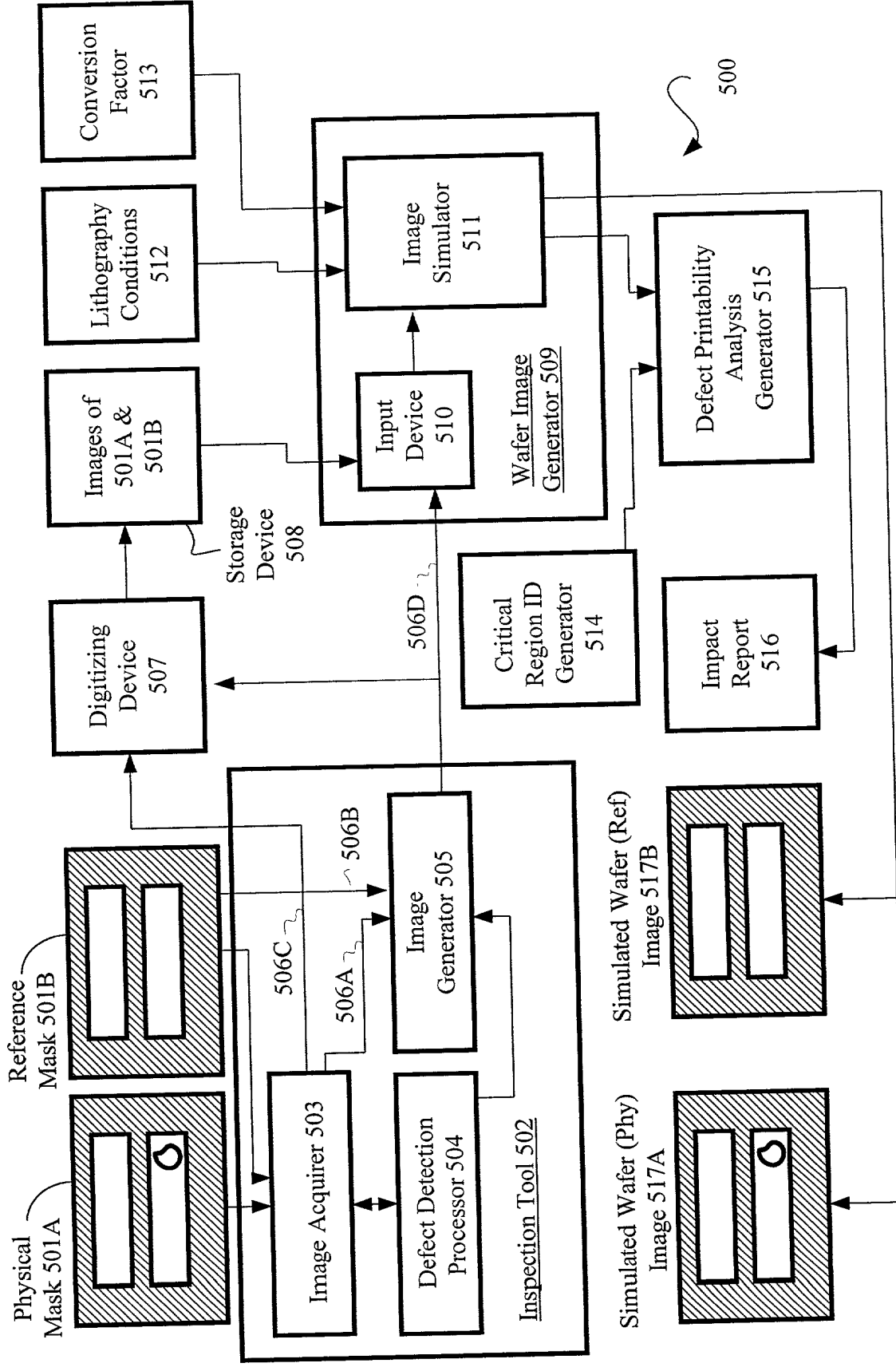


Figure 5

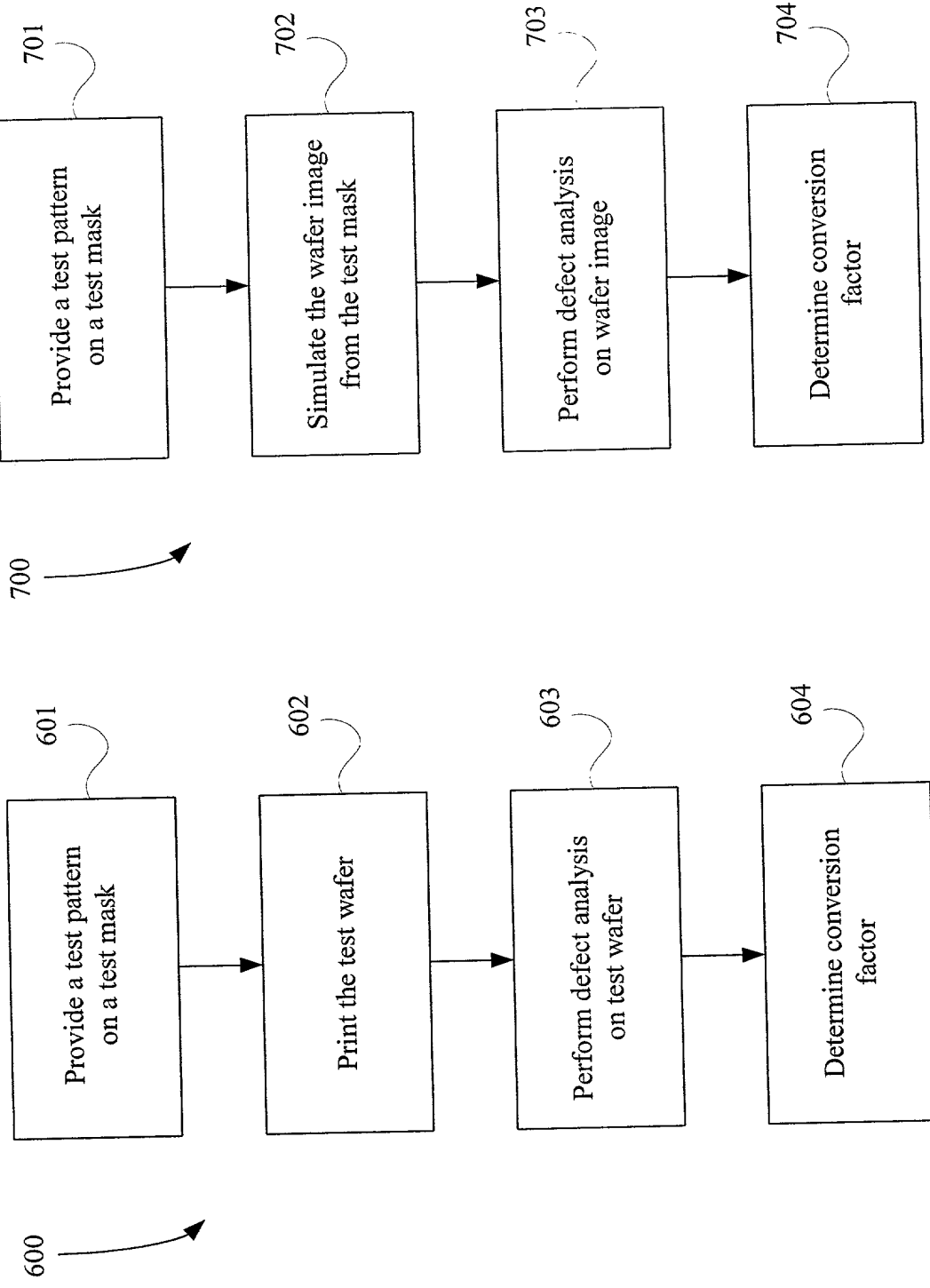


Figure 6

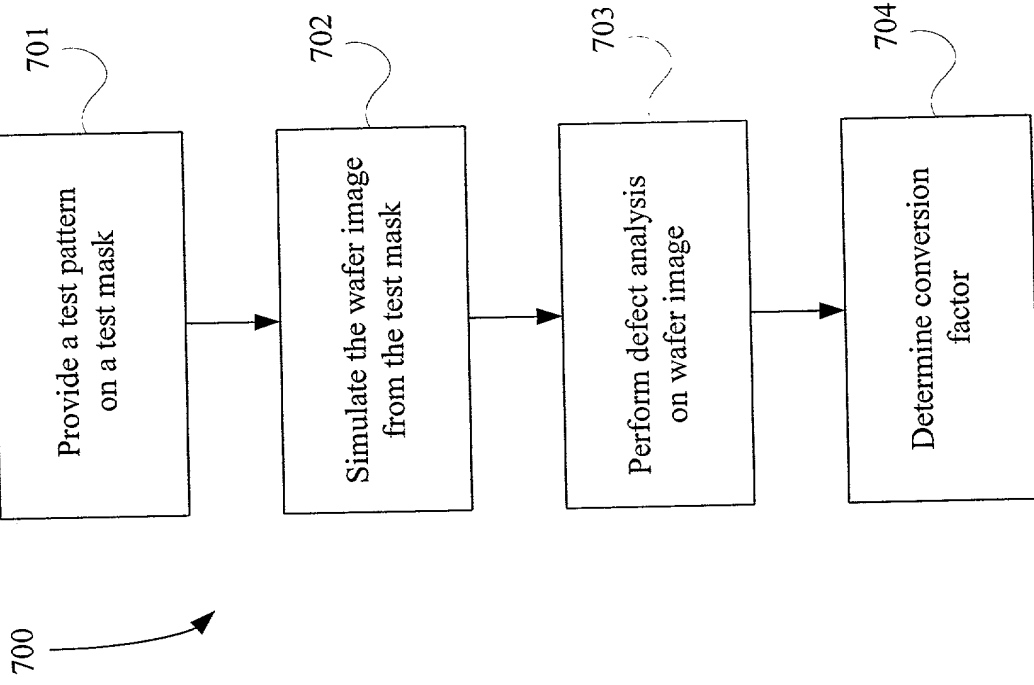


Figure 7

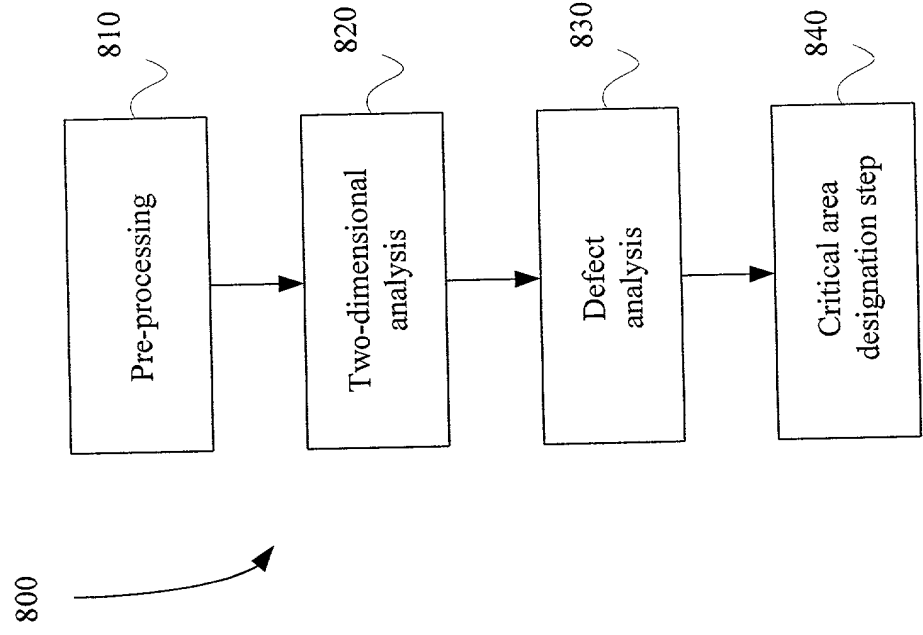


Figure 8A

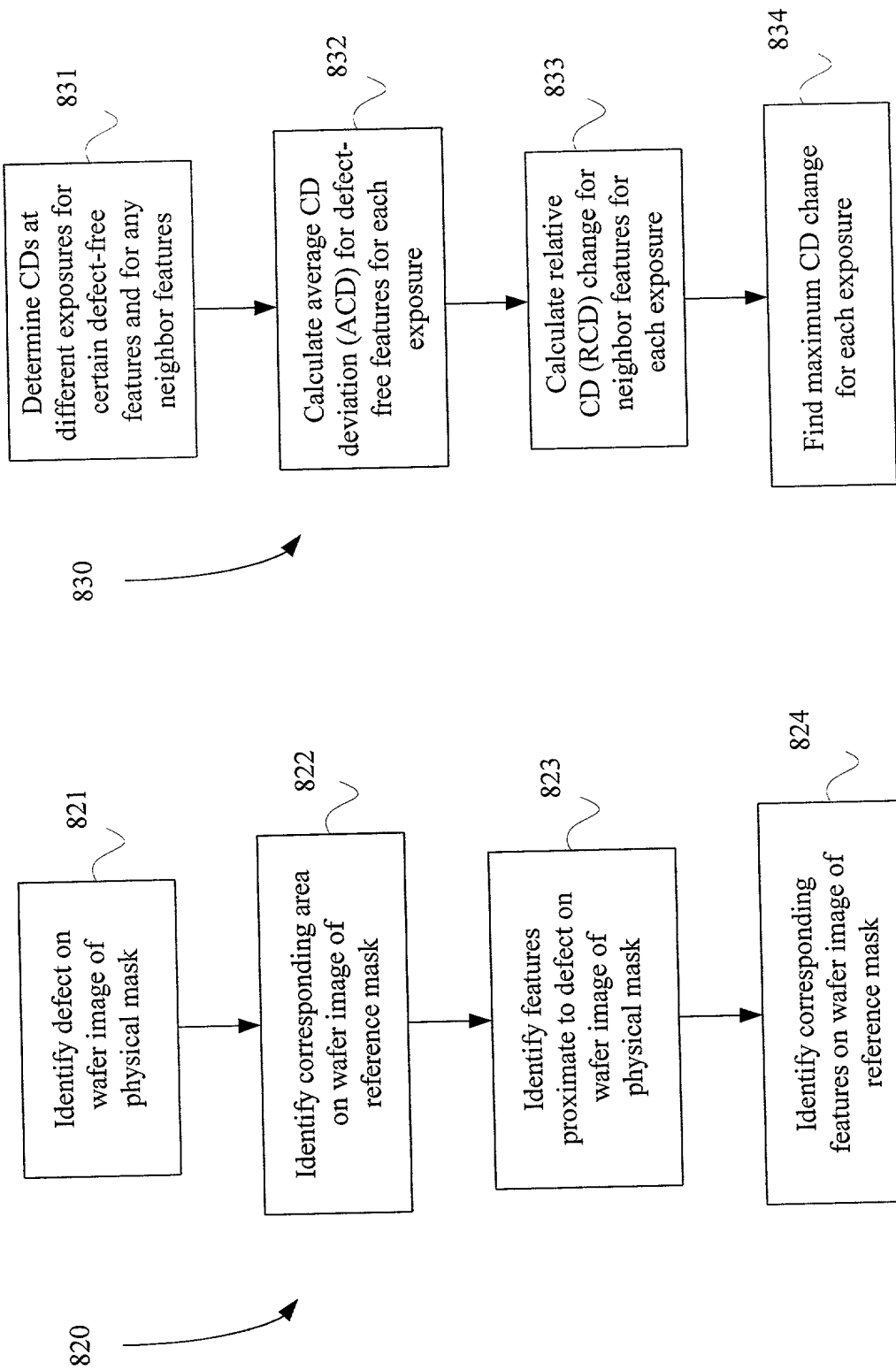


Figure 8C

Figure 8B



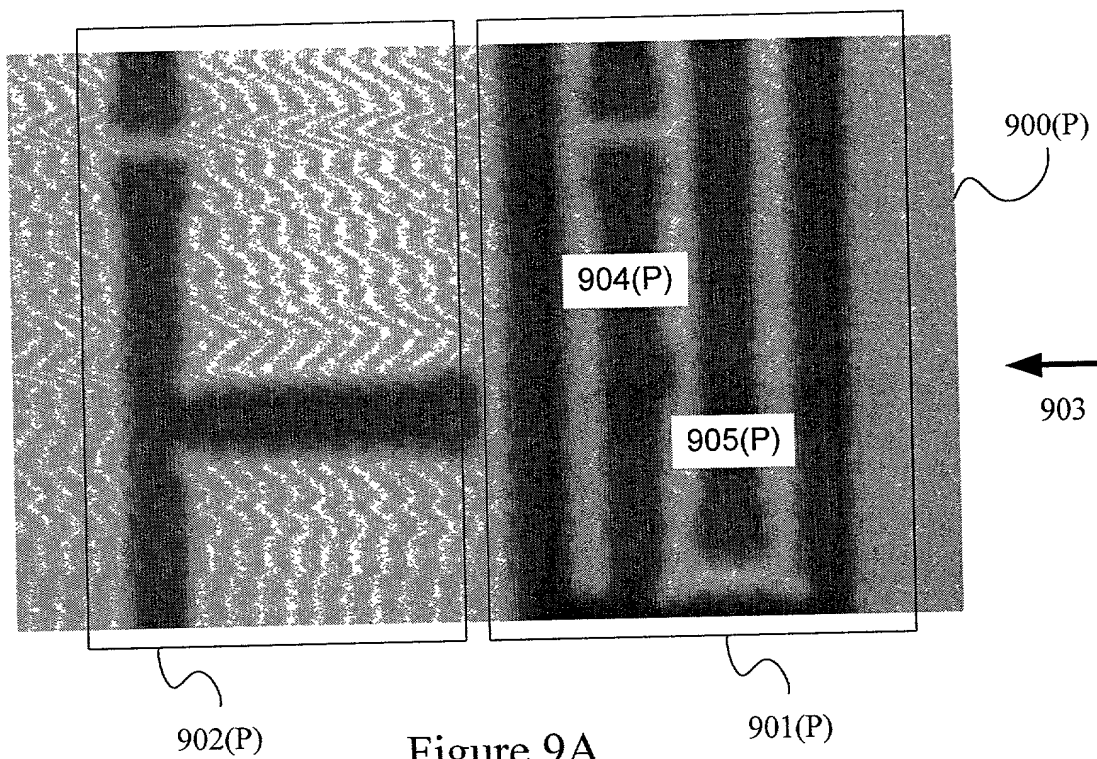


Figure 9A

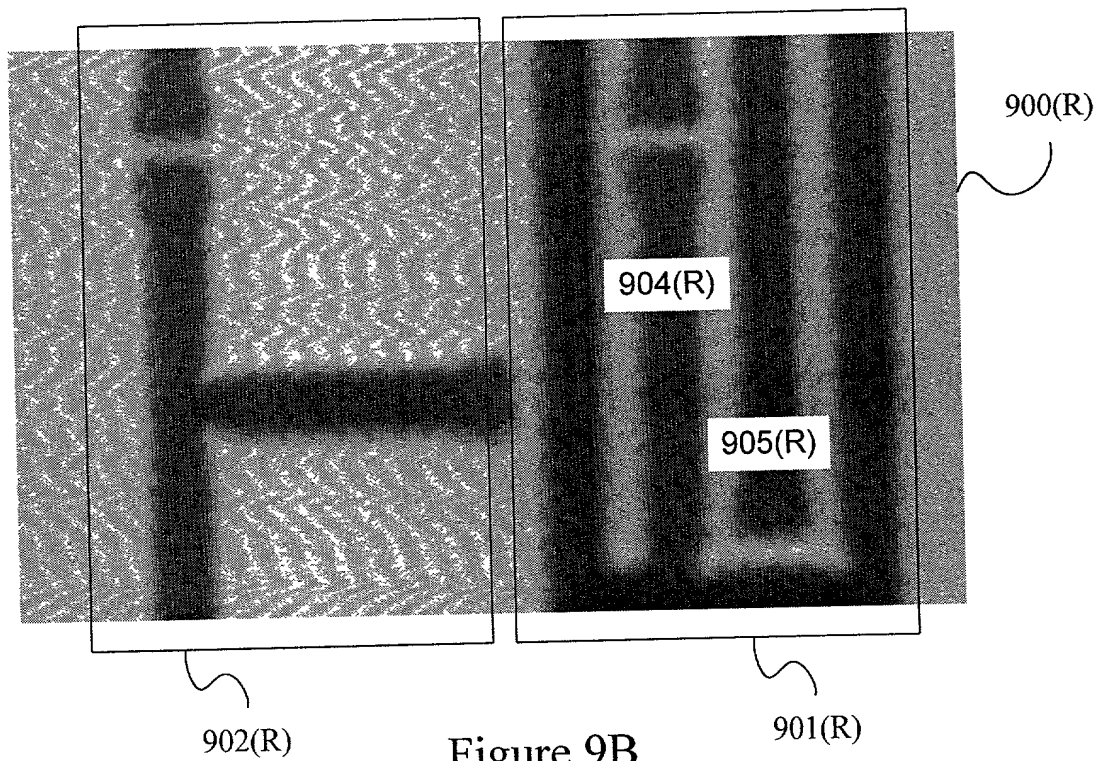
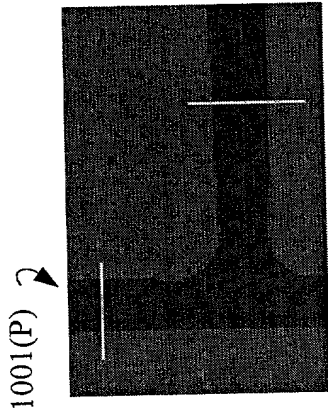


Figure 9B



1001(P)

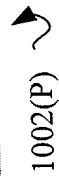
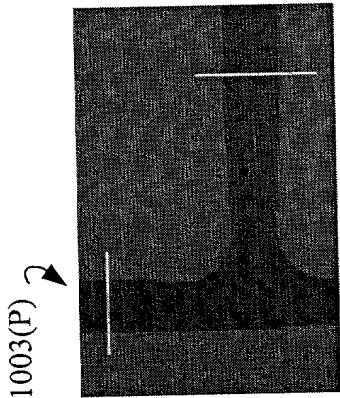


Figure 10A(1)



1003(P)

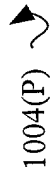
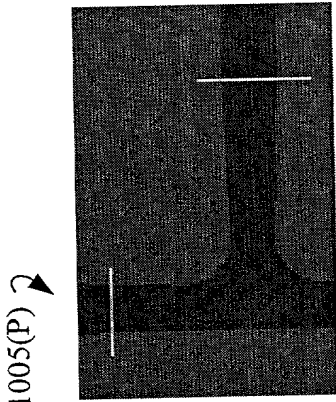


Figure 10A(2)



1005(P)

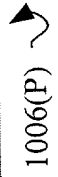
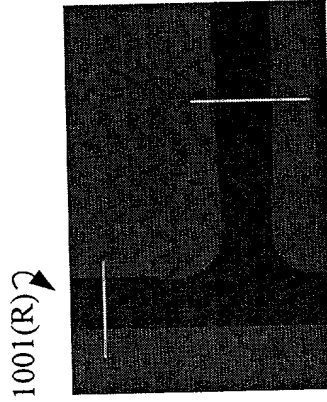


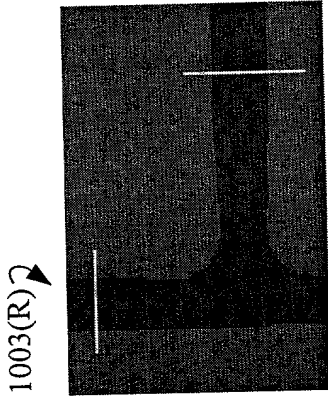
Figure 10A(3)



1001(R)



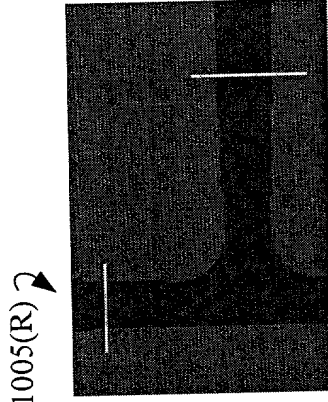
Figure 10B(1)



1003(R)



Figure 10B(2)



1005(R)



Figure 10B(3)

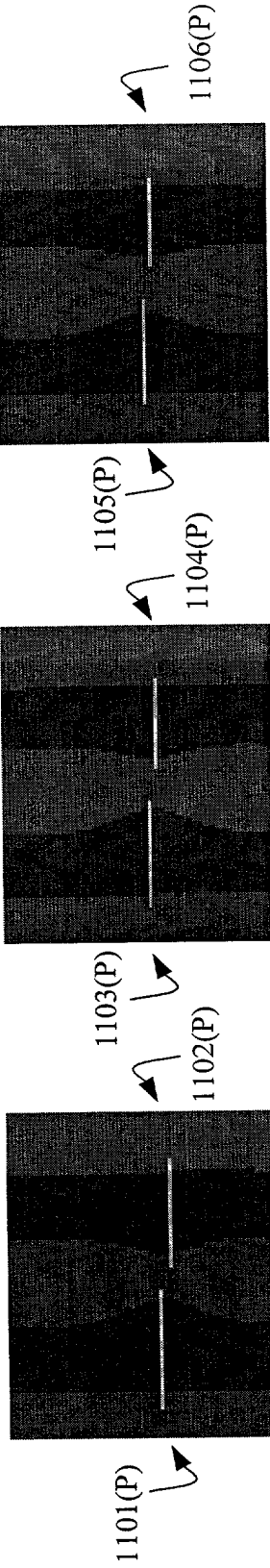


Figure 11A(1)

Figure 11A(2)

Figure 11A(3)

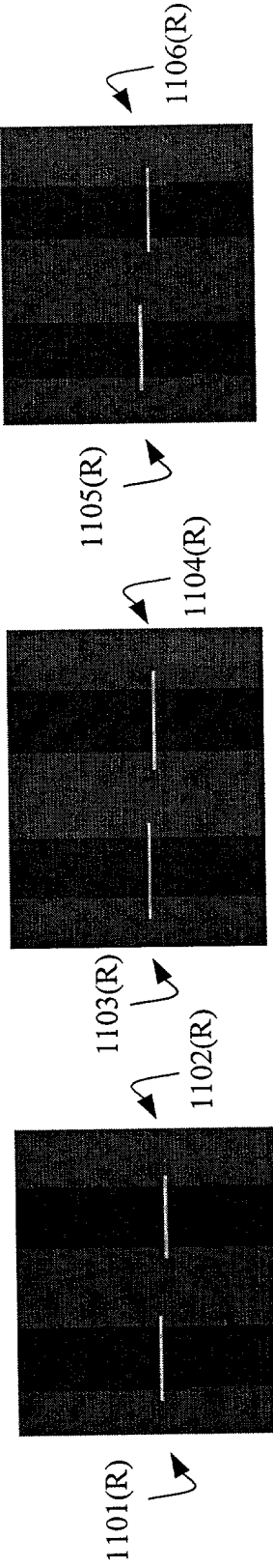


Figure 11B(1)

Figure 11B(2)

Figure 11(3)

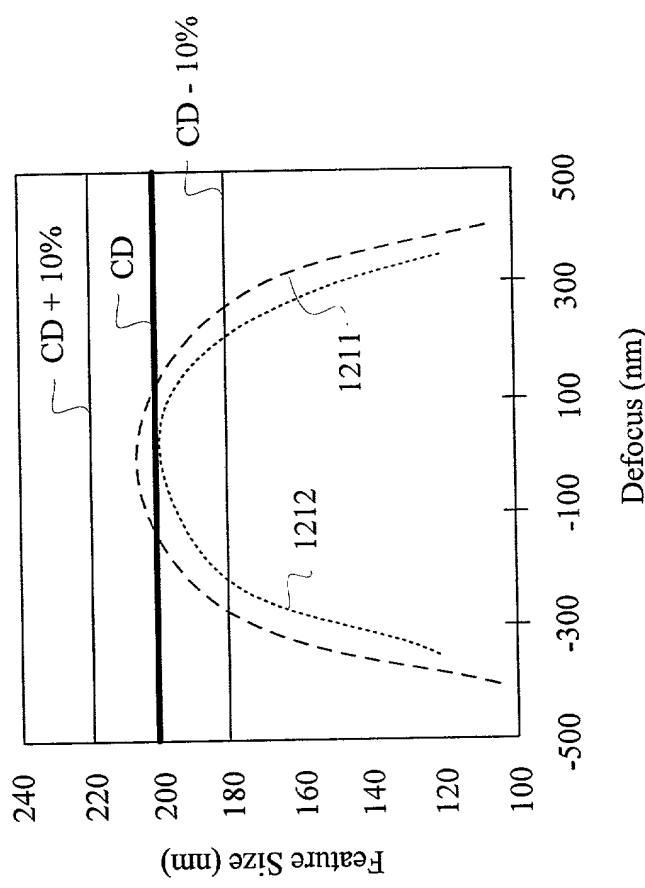


Figure 12A

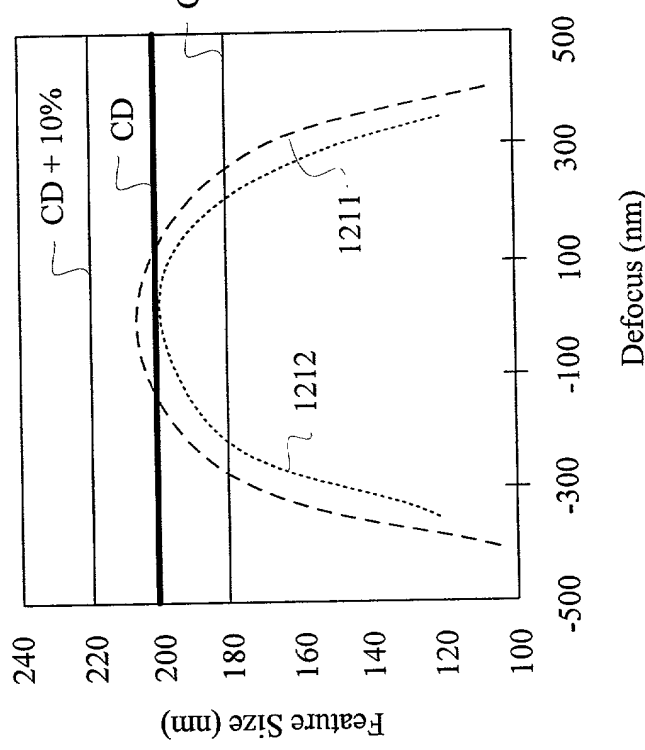


Figure 12B

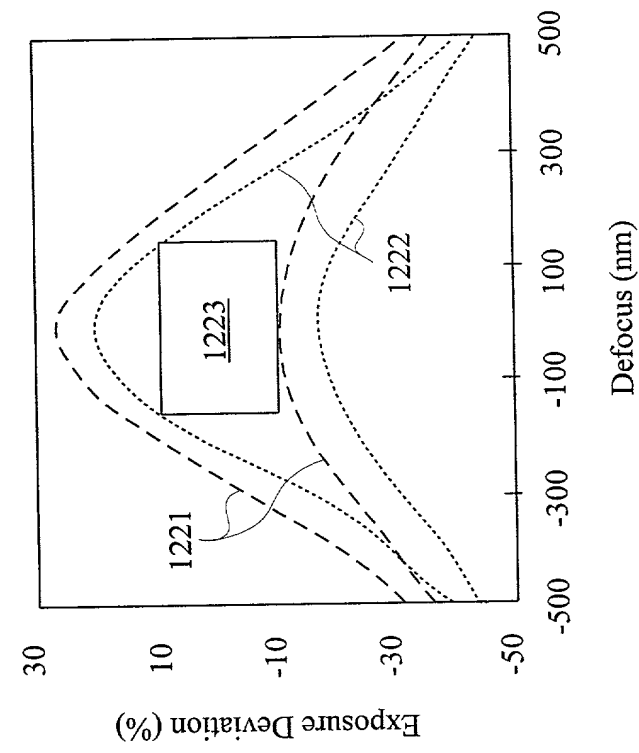


Figure 12C

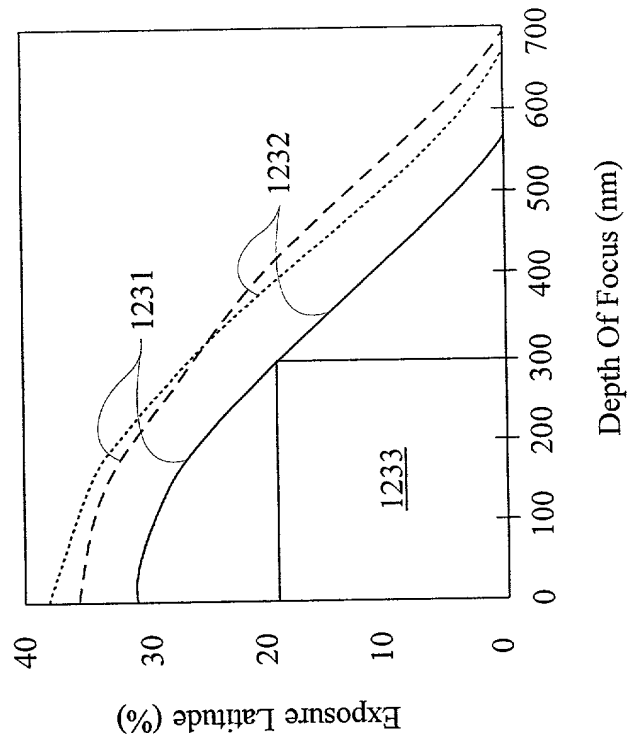


Figure 12D

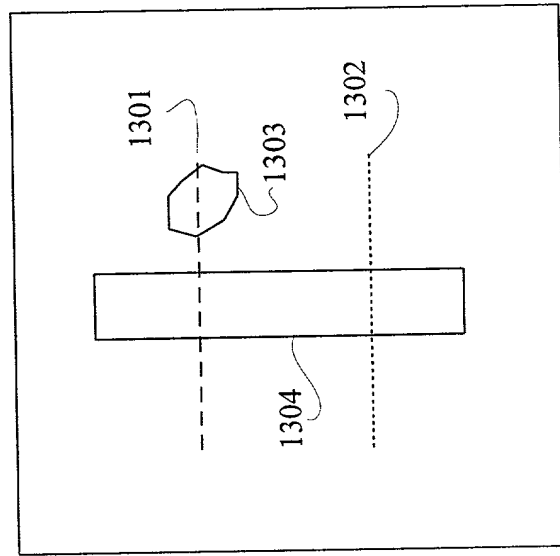


Figure 13A

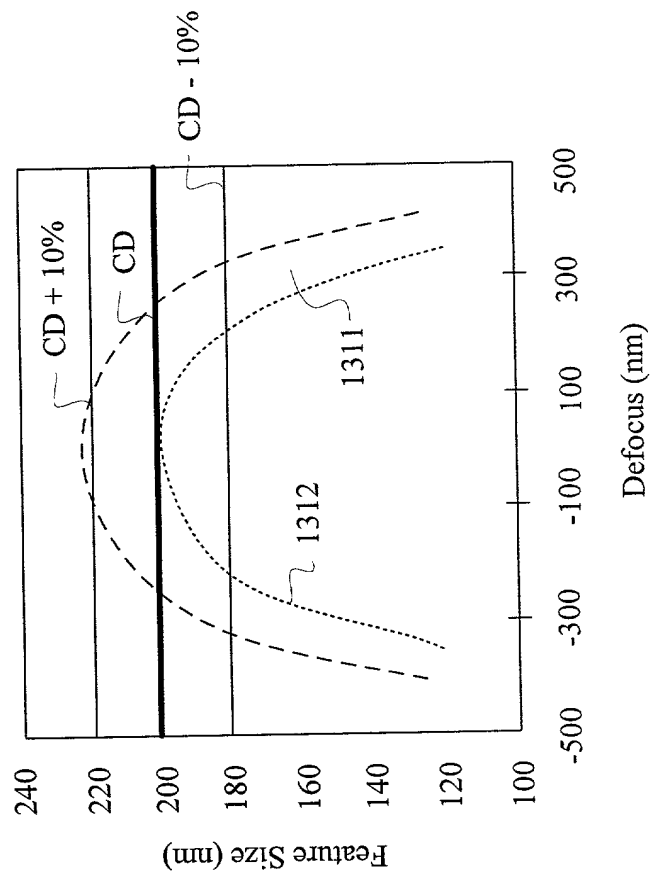


Figure 13B

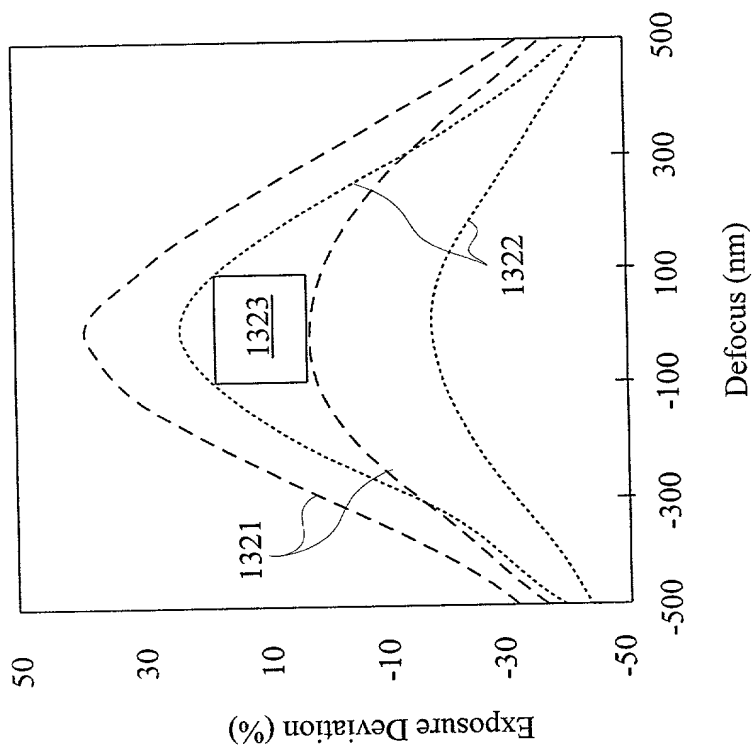


Figure 13C

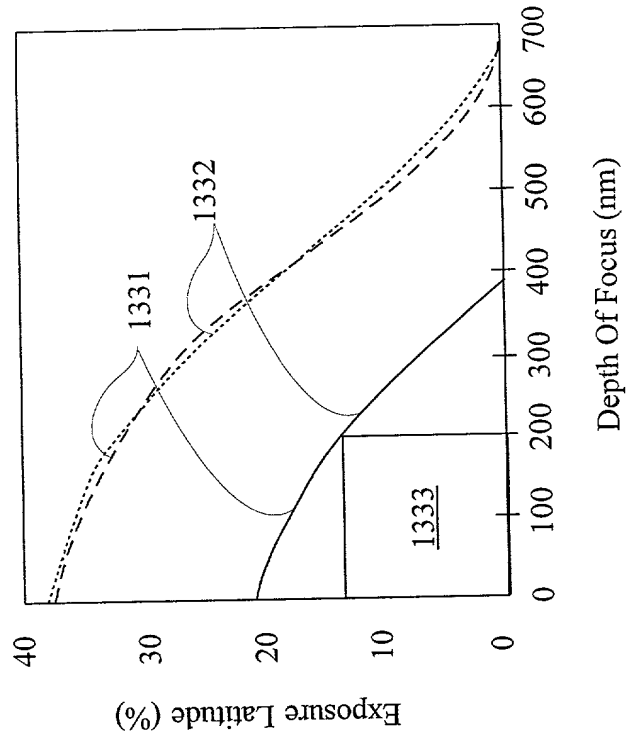


Figure 13D

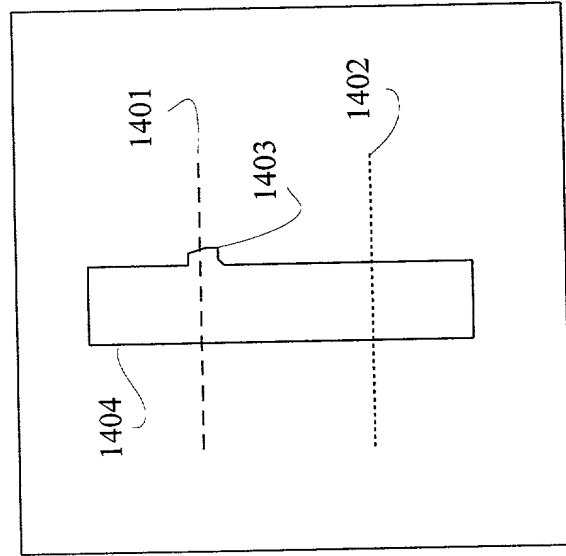


Figure 14A

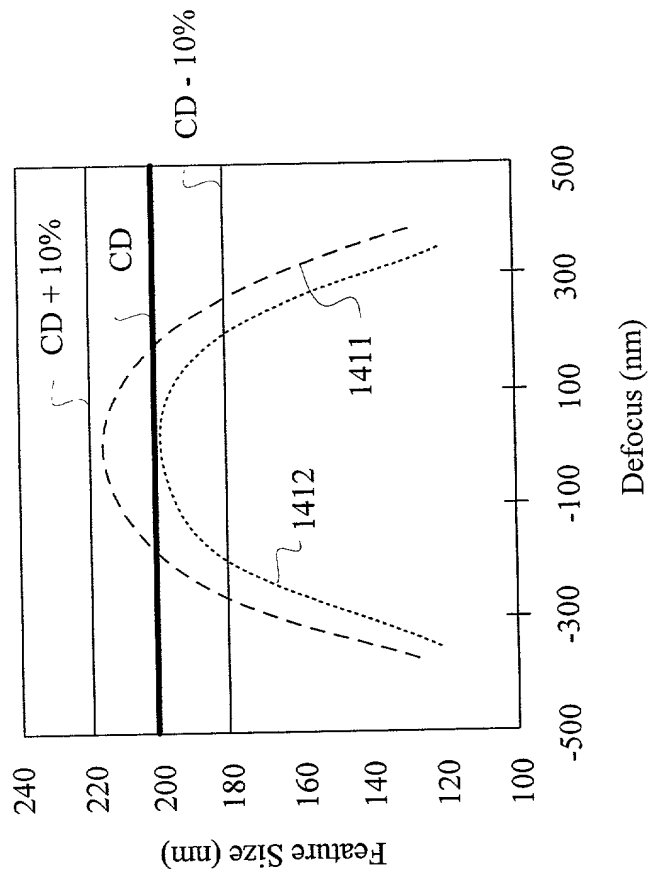


Figure 14B



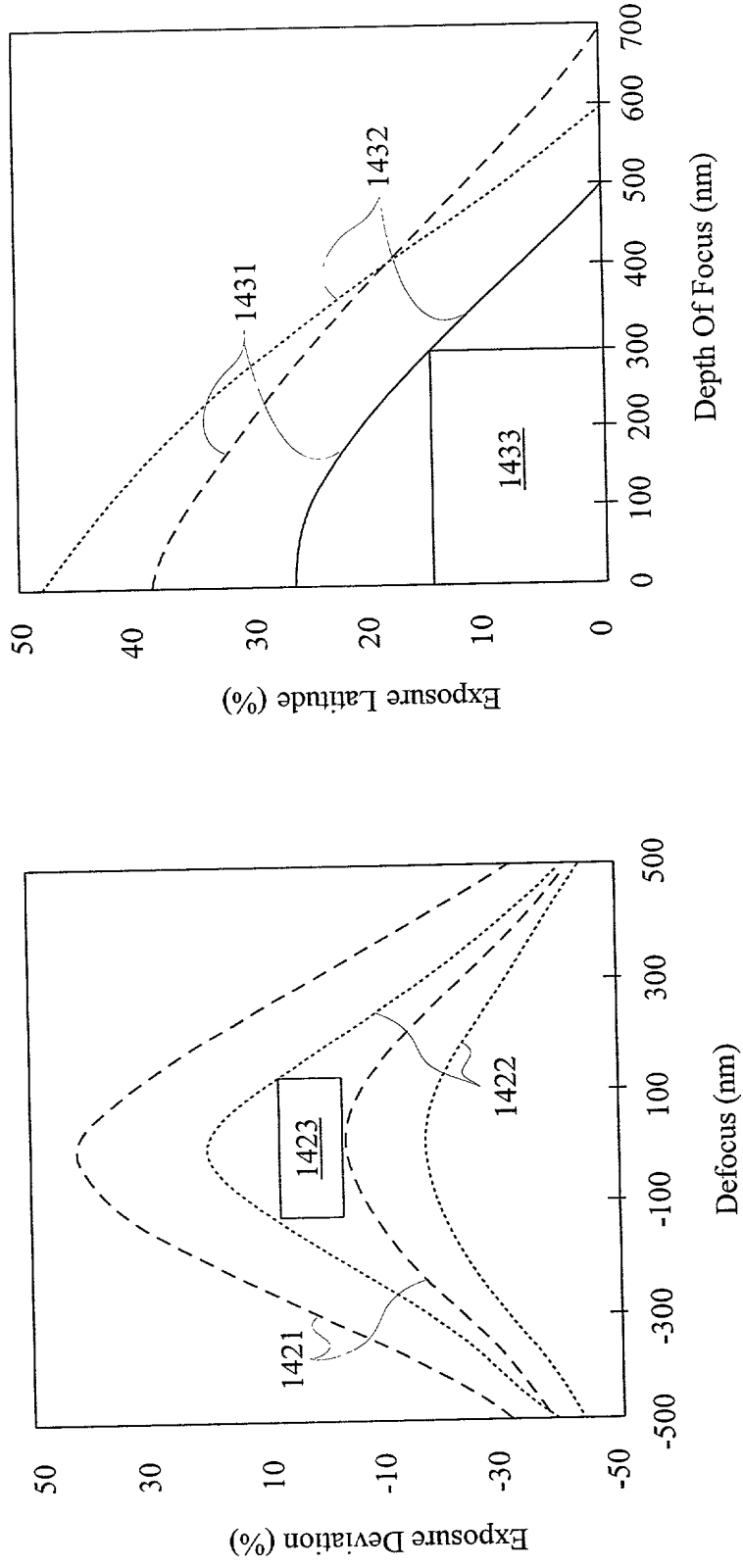


Figure 14D

Figure 14C

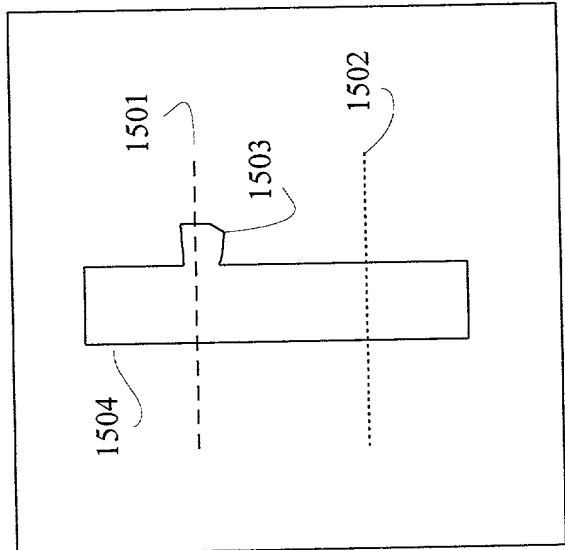


Figure 15A

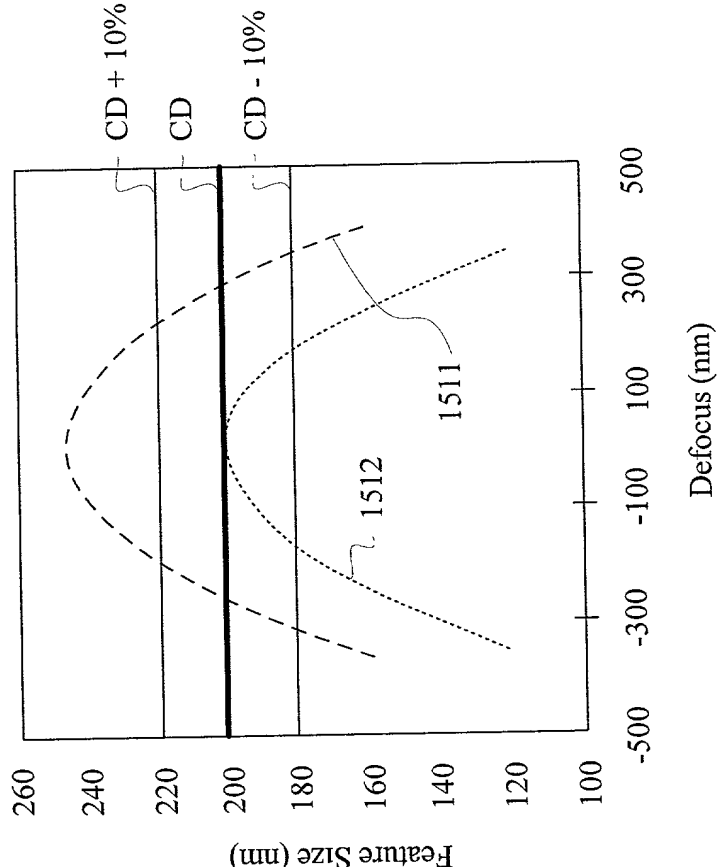


Figure 15B

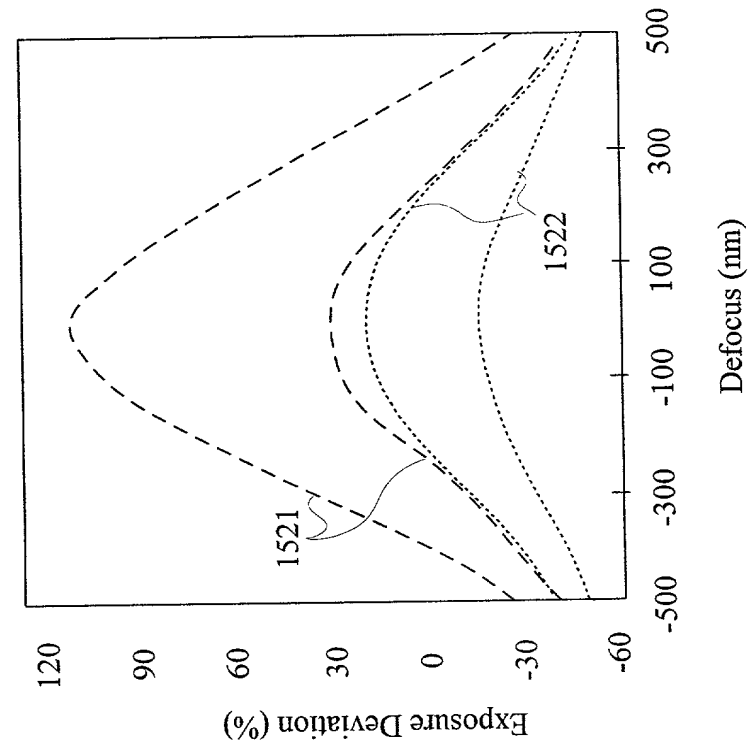


Figure 15C

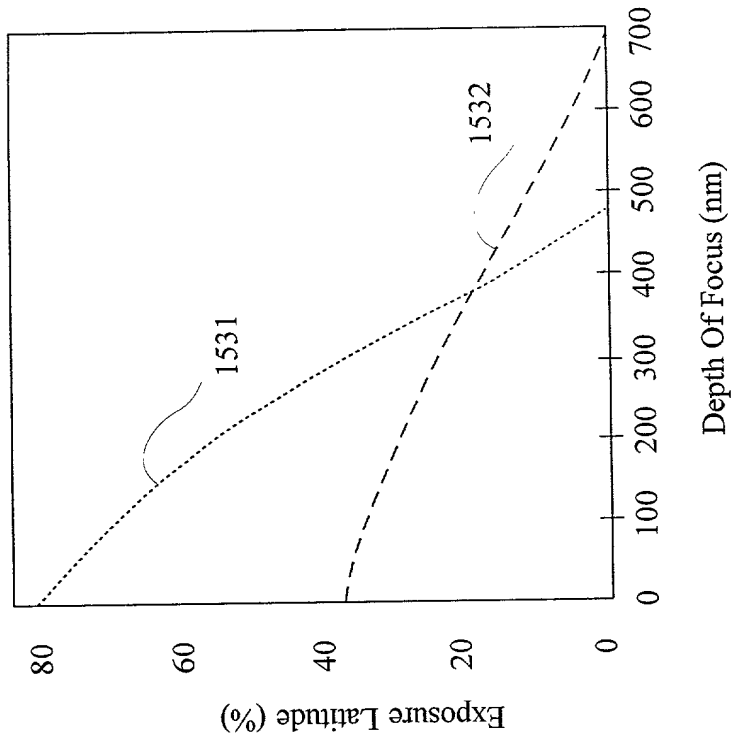


Figure 15D

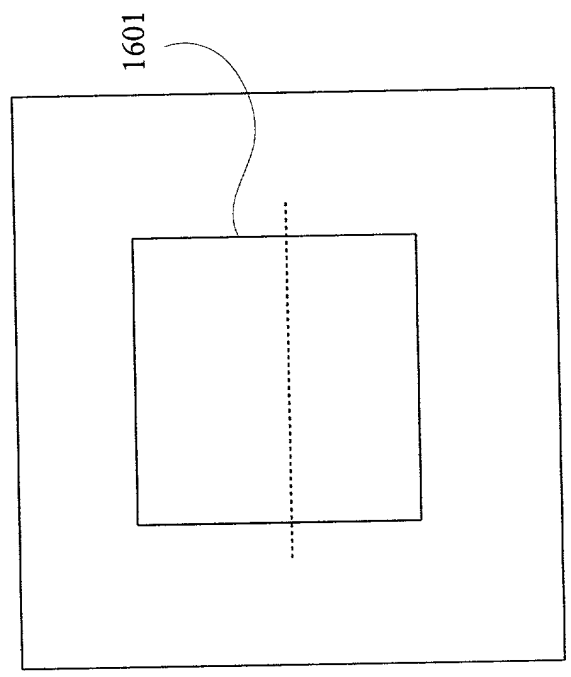


Figure 16A

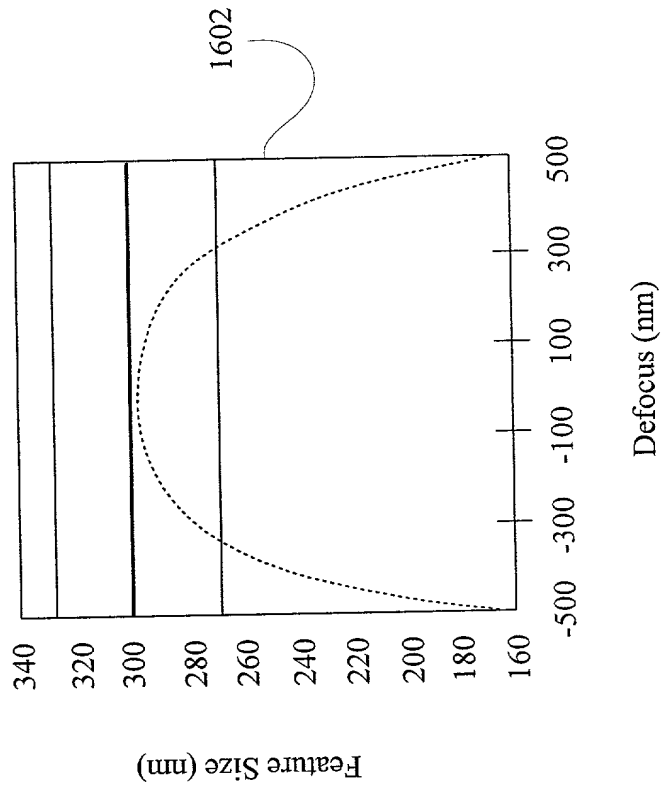


Figure 16B

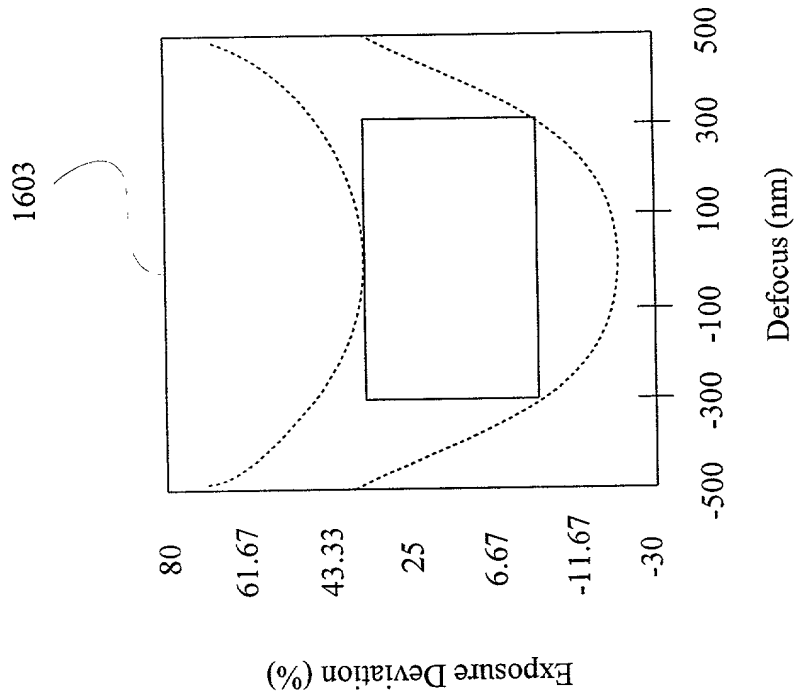


Figure 16C

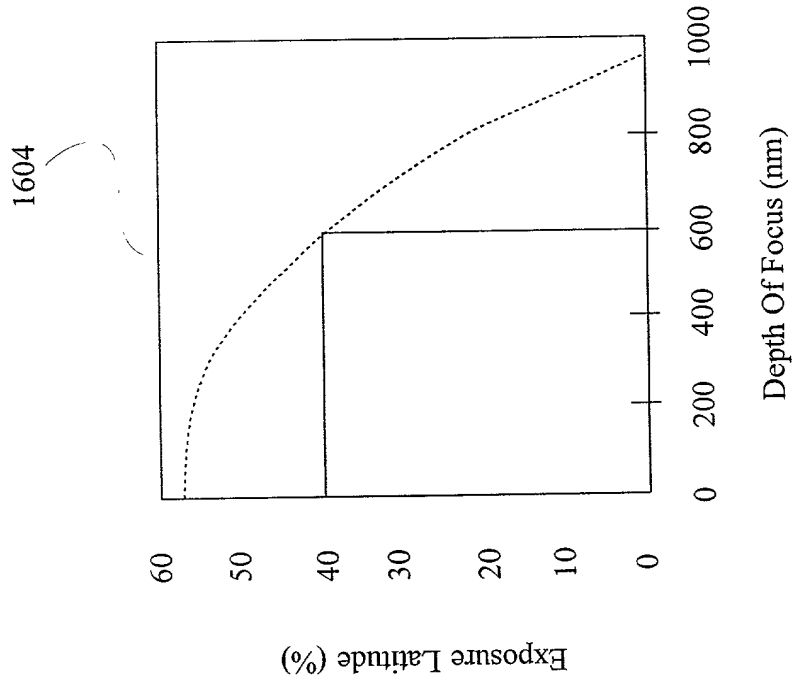


Figure 16D

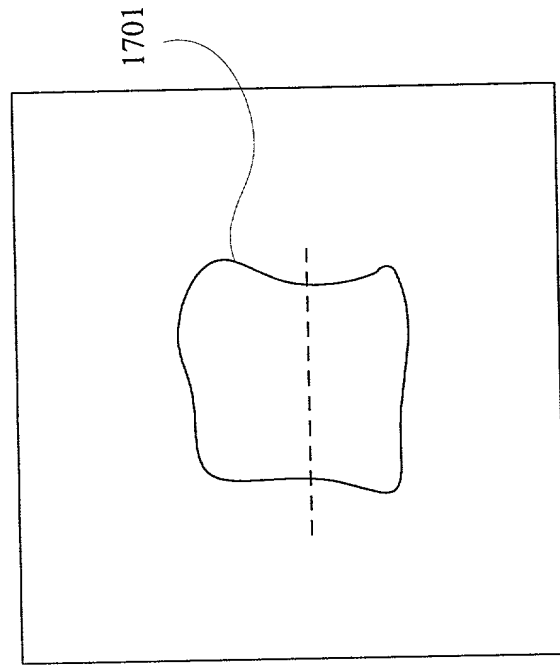


Figure 17A

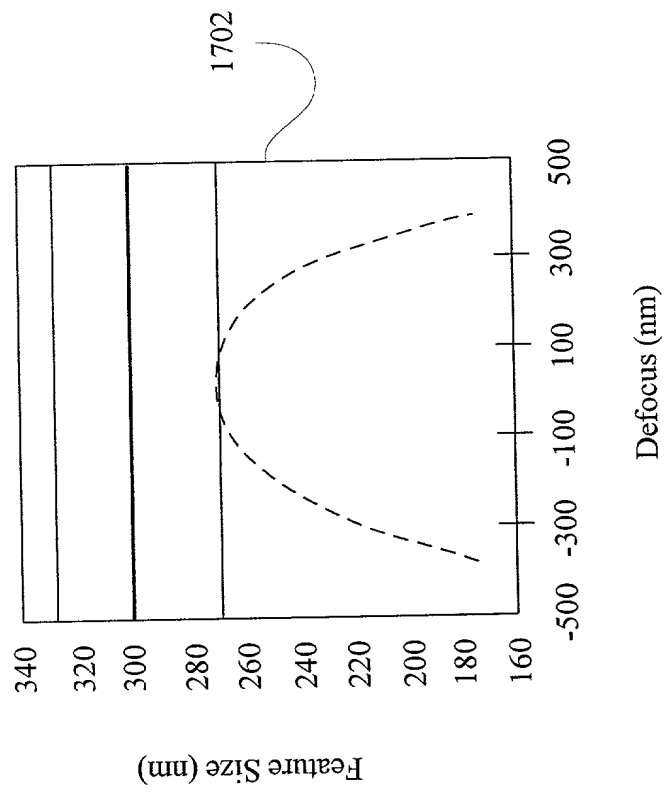


Figure 17B

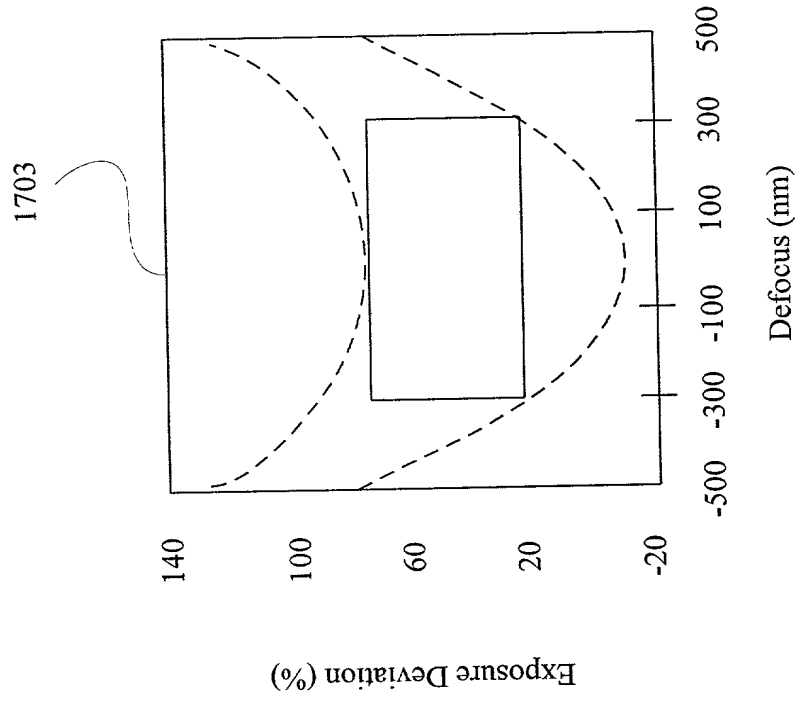


Figure 17C

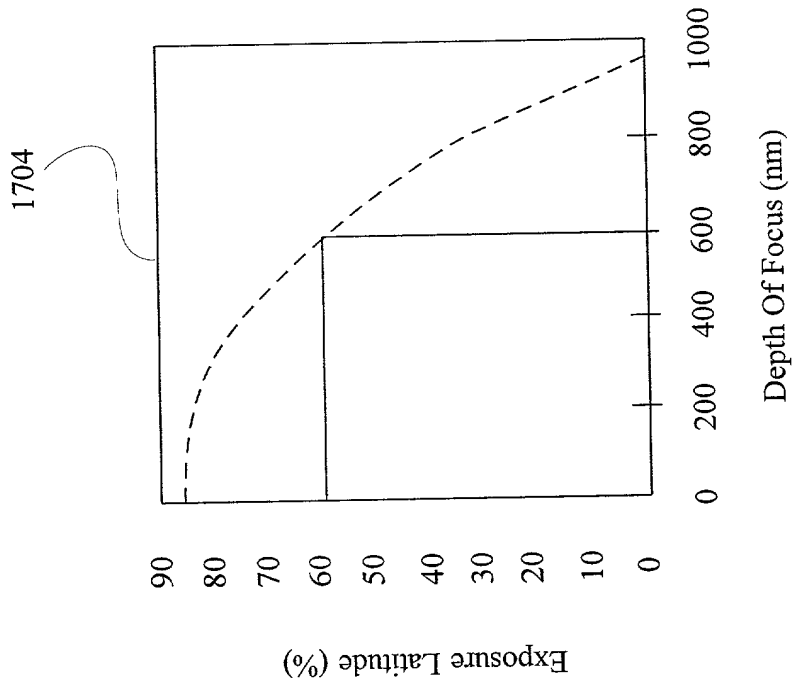


Figure 17D

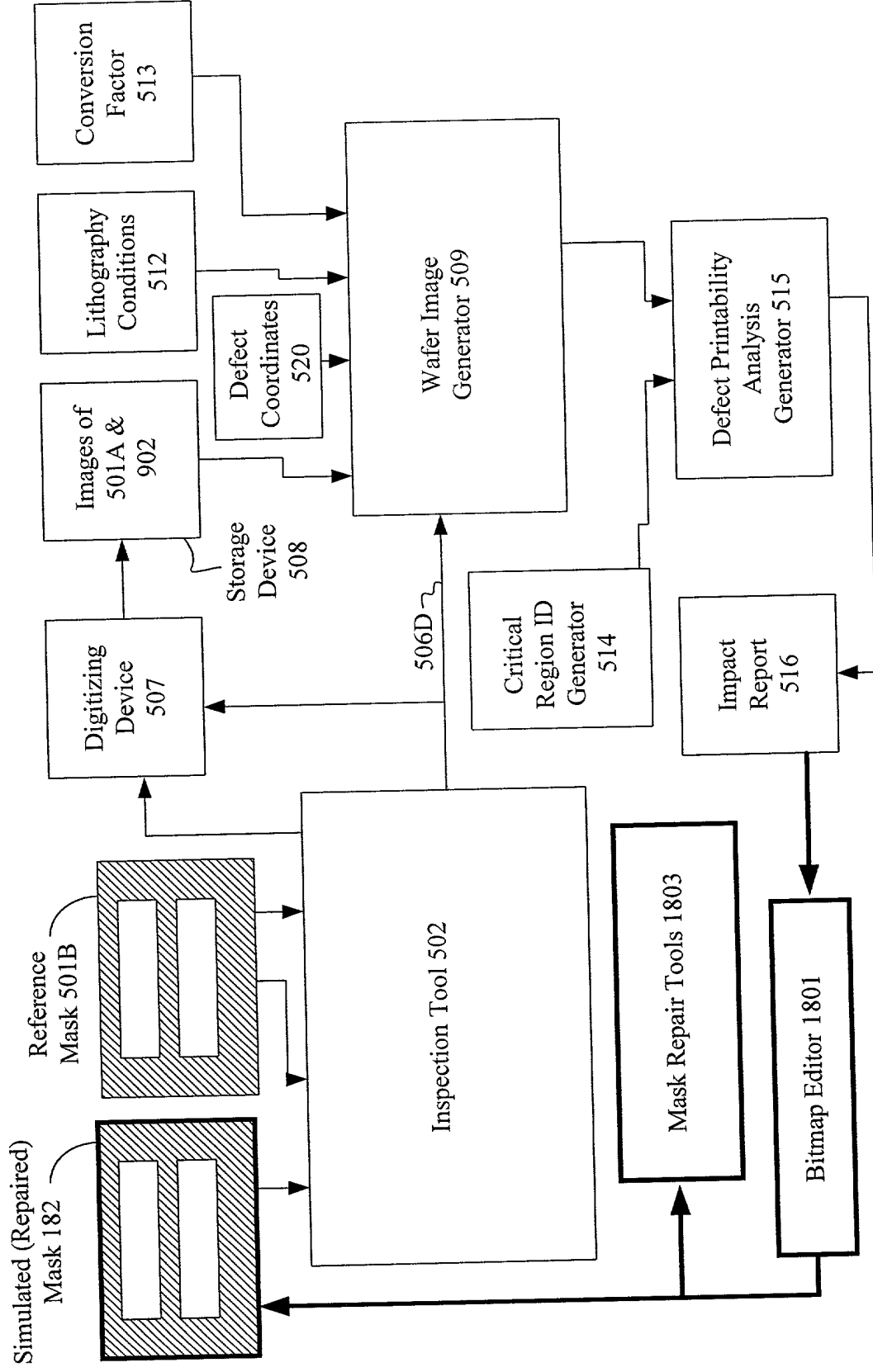


Figure 18



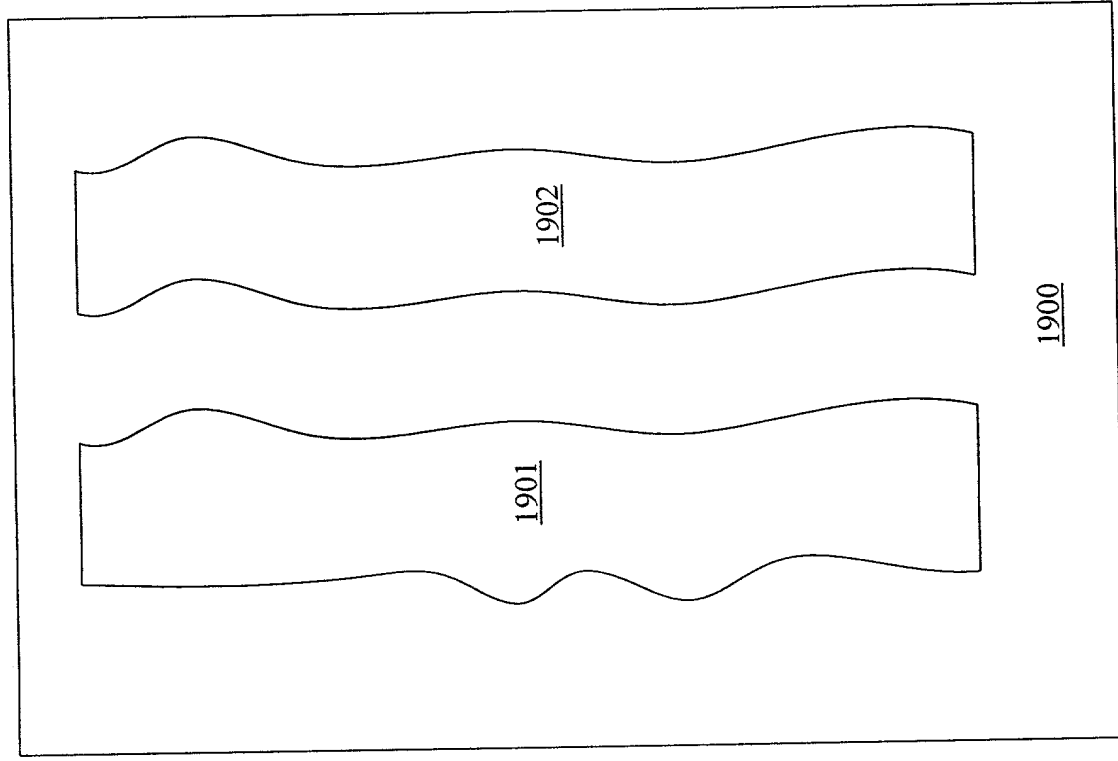


Figure 19A

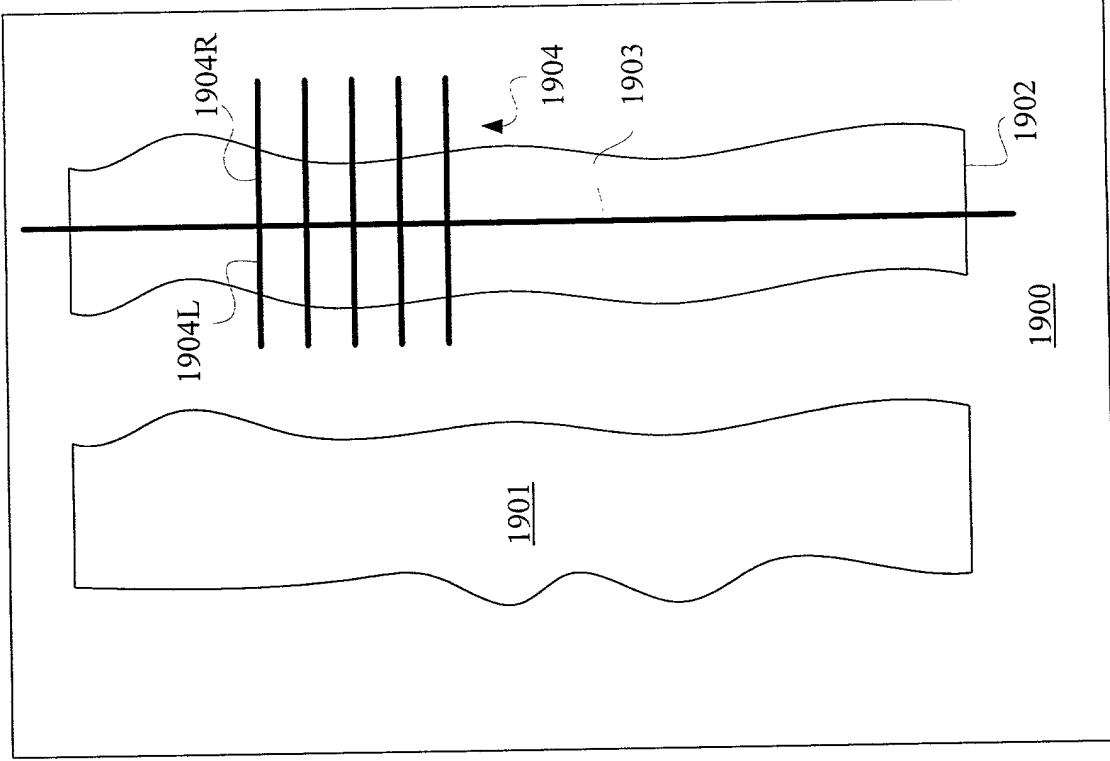


Figure 19B

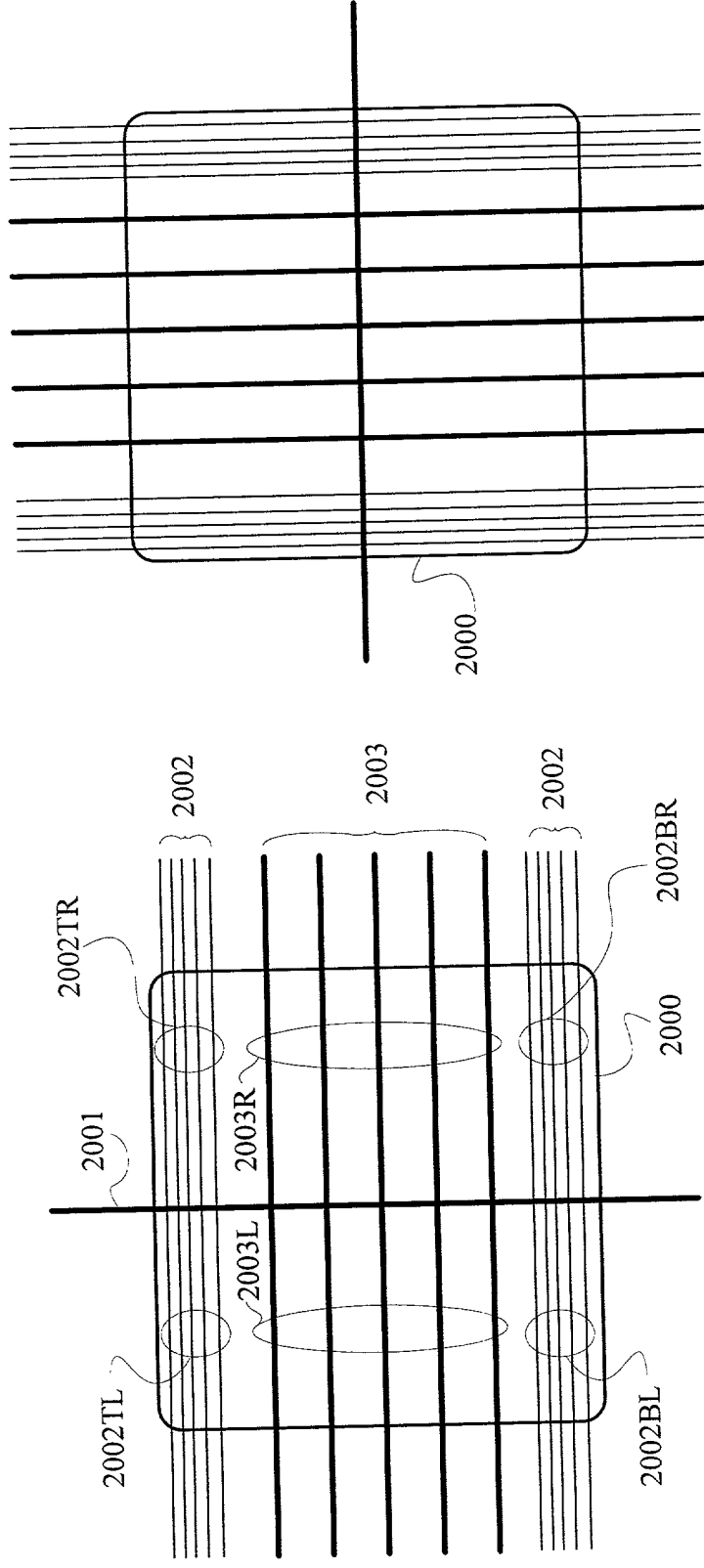


Figure 20B

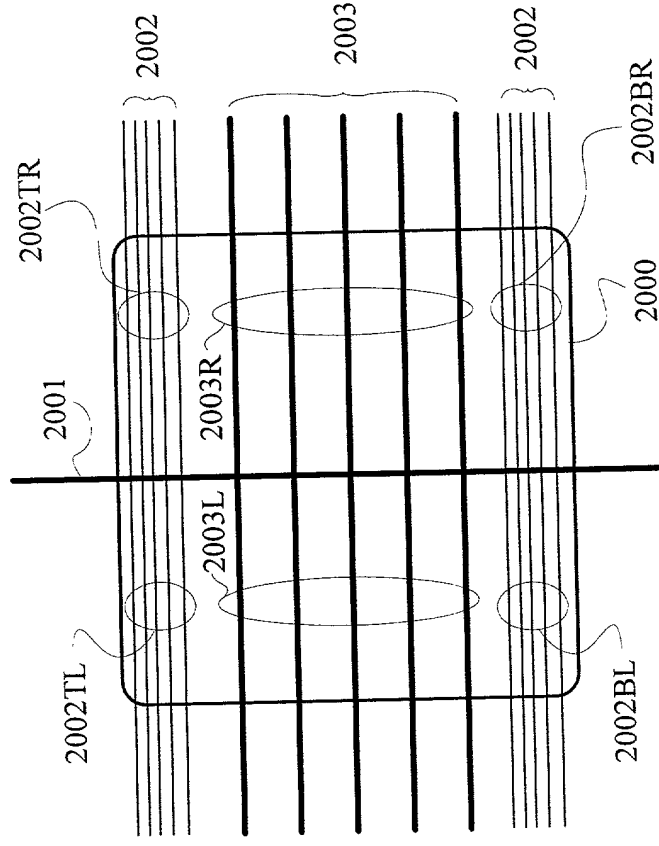


Figure 20A